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Hermetic Encapsulation of Nanoenergetic Porous Silicon Wafer by Parylene

**by Eugene Zakar, Wayne Churaman, Collin Becker, Bernard Rod,
Luke Currano, and John Conrad**

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<p>14. ABSTRACT Parylene film is attractive for hermetic encapsulation of porous surfaces, including energetic materials, and for the protection of integrated circuits on large-diameter silicon substrates. Achieving uniformity and repeatability of chemical vapor deposited (CVD) parylene film on large-diameter wafers in a batch system is challenging. The difficulties are related to improper selection of the wafer attachment apparatus in the chamber, and the poor coating repeatability from run to run is attributed to wafer volume changes in the CVD chamber. We discuss hardware modifications and preparation methods that improve the predictability, uniformity, and adhesion of the parylene film on nanoporous silicon surfaces. Atomic force microscopy (AFM) can determine surface roughness and distinguish differences in nanoporous silicon etched surfaces. Energetic materials that are hygroscopic in nature need to be protected from the environment during storage to improved ignition lifetime. Parylene film is an effective moisture barrier for nanoporous-scale material applications. We tested the adequacy and lifetime of parylene protection layer for a nanoenergetic device and found the shelf life can be extended in environments with greater than 80% humidity.</p>				
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1. Introduction/Background

Parylene is considered by many to be the best coating protection for surfaces, components, and devices in a wide variety of industries. Parylene coatings created by a chemical vapor deposited (CVD) method can be completely conformal and pinhole free. For many years, the electronics industry has been using parylene as a coating for electrical boards, but recently found they were having a great difficulty achieving uniformity and repeatability of CVD parylene films^{1,2} on large-diameter wafers in a batch system. In their process, the same holding apparatus inside the CVD chamber was used repeatedly, but not filled to capacity from run to run. Doing this causes changes in the amount of surface being exposed when the parylene material is being deposited inside the chamber. Also, there are difficulties concerning uniformity within a large-surface wafer, which are related to the improper selection of the wafer holding apparatus. In batch production processes in the semiconductor industry, cassettes are traditionally used to hold as many as 25 wafers at a time. We found that cassettes produce non-uniform coatings due to edge effects on the wafers. We learned that wafers need to be individually placed on a flat carrier such that nothing comes close to its edges, and that the separation between the wafers needs to be much greater than the current 5-mm tolerances. Figure 1 illustrates a) a conventional cassette wafer holder with silicon wafers and b) a flatbed carrier we designed in-house.

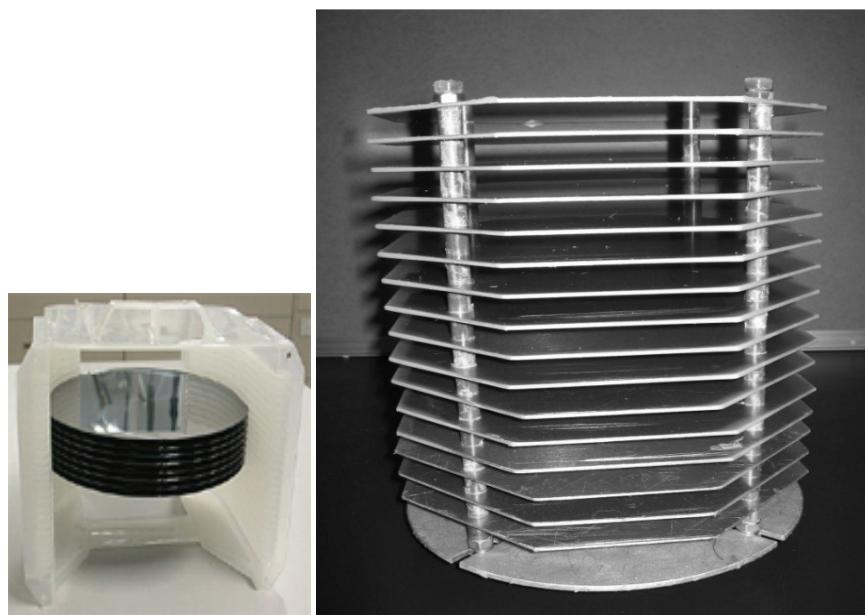


Fig. 1 Picture of a) cassette holder with wafers and b) flatbed carrier

The uniformity and surface appearance of a parylene-coated wafer can change dramatically depending on how it sits in the deposition chamber. Figure 2 illustrates the surface appearance of parylene coated on a 100-mm-diameter silicon wafer solely based on the wafer attachment

methods. Differences in the fringe patterns are shown for a wafer held by a conventional cassette (Fig. 2a) and by a flatbed carrier (Fig. 2b). Parylene is normally transparent, but when held up against a reflecting light source, optical fringes in the form of rainbow colors appear and represent variations in the coating thickness. Each color band, in this case, roughly represents approximately a 10-nm change in film thickness. A large number of fringes translate to large variations in the coating thickness, while a small number represent a more uniform coating. The color fringes in the photographs were artificially enhanced to illustrate the film coating characteristics. We found that wafers placed in close proximity to objects (edge effects) can change the arrival rate of the chemical vapor deposited parylene inside the CVD chamber. After implementation of a flatbed carrier inside the CVD system, the number of fringes was significantly reduced and the patterns became equally spaced, as depicted in Fig. 2b. Later in the report, we discuss how changing the number of wafers and their relative positions inside the CVD chamber can affect coating thickness.

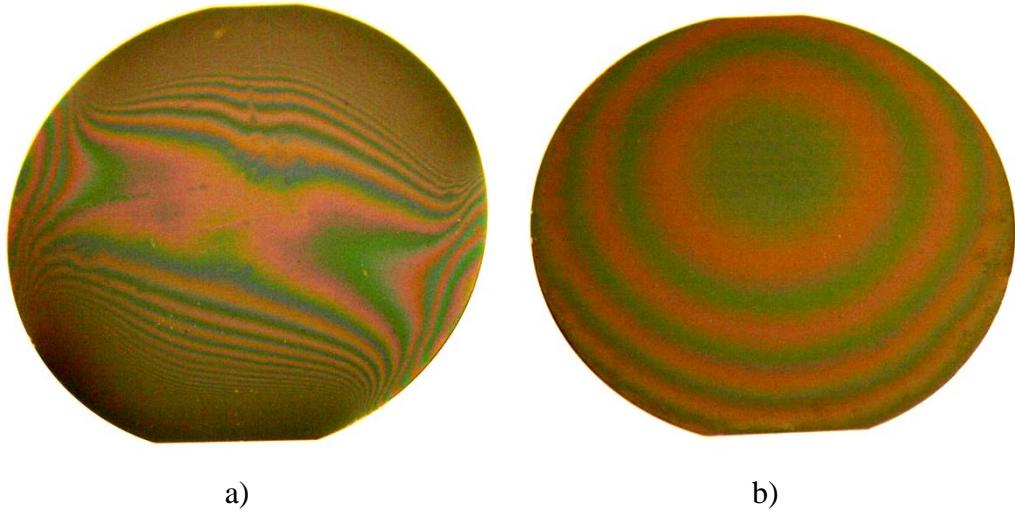


Fig. 2 Reflected light fringe patterns on a parylene-coated wafer created in a) conventional cassette and b) flatbed carrier

The number of applications for parylene has grown dramatically over the past several years and new applications are being discovered. We highlight the important parameters for effectively applying a parylene coating onto a nanoenergetic porous silicon (PS) substrate. Parylene is the trade name for a variety of CVD polymers that come in N, C, and D types, each having their own unique electrical and physical properties. The various chemical structures⁵ are shown in Fig. 3. Parylene N has the most basic structure, but we use parylene C, because it has an additional chlorine atom on the benzene ring, which produces the unique physical properties of particularly low moisture and low gas permeability, and it has the fastest deposition rates among this group of polymers.

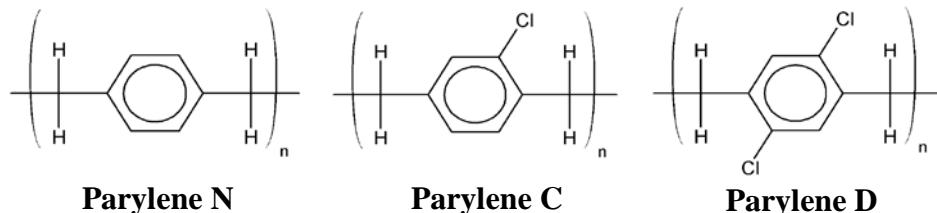


Fig. 3 Chemical structures for different types of parylene

We describe the necessary preparations and improvements to equipment, and process highly reliable and uniformly hermetically sealed integrated circuits and devices on 4-in-diameter wafer substrates. The same principles can be extended to larger chamber and wafer configurations. Figure 4 shows a block diagram of a Union Carbide 10C deposition system currently in use at our laboratory.

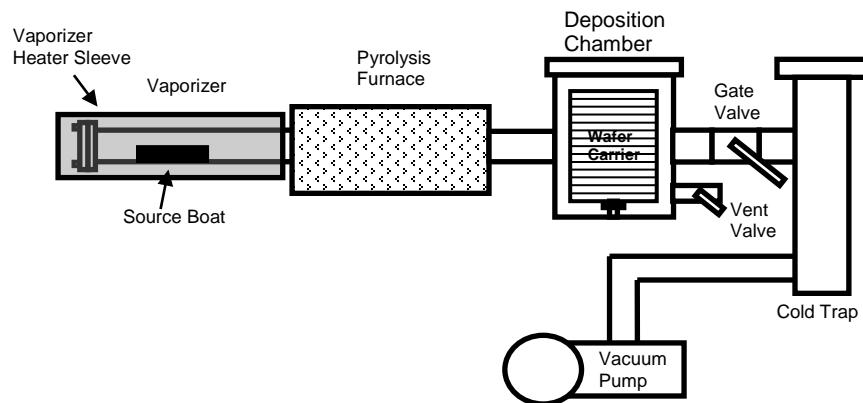


Fig. 4 Block diagram of the parylene CVD system

In the preparation stage, a chemical precursor “dimer” is appropriately weighed and placed into a source boat, which is inserted into the vaporizer tube, which is then pumped down to approximately 67 Pa (0.5 Torr). During the actual process, the dimer is vaporized at 175 °C. The dimer vapor then enters the furnace where it undergoes pyrolysis at 670 °C, forming a monomer vapor. Finally, the monomer vapor passes into the deposition chamber as a clear polymer film at room temperature. Because the deposition takes place from a gaseous source, the vapor-deposited parylene layer is extremely dense and provides an excellent conformal coating on complex surfaces. Our existing deposition chamber is approximately 10 inches in diameter and 12 inches high. A liquid nitrogen cold trap, located between the vacuum pump and deposition chamber traps, prevents the parylene vapors from clogging the vacuum pump. Although this system was one of the first commercially available parylene deposition systems, its configuration is virtually identical to many of the newer systems currently on the market but without the fully automated operating functions.

2. Experimental

2.1 Film Repeatability

Researchers have encountered a great difficulty in predicting parylene film thickness in batch processes when the number of wafers loaded into the chamber changes from run to run. The explanation is simple, but not obvious at first. The amount of exposed surface (effective surface area) inside an empty chamber changes with the addition of objects. When a fixed weight of dimer is loaded into the vaporizer, it yields the same coating thickness as long as the total surface area inside the chamber remains constant. Adding more objects means more dimer is required to compensate for the added difference in surface area. An improved approach to solve this would be to hold the total effective surface area inside the CVD chamber as constant as possible from run to run. One way to accomplish this is to design a carrier with an enormous amount of exposed surface plates, so the total surface parameter can be held constant. The plates should not be comprised of perforated surfaces. As long as the same carrier is used between runs, the parameters remain constant. Thus, a custom fabricated set of flatbed carriers illustrating this concept was assembled. The total effective exposed surface area inside the chamber, including the carrier, remains relatively constant no matter how many wafers are added or subtracted between runs. The sidewall of each wafer is only 0.5 mm and does not add to the total exposed surface area inside the chamber. The separation between the wafers is also much greater than the tolerances found in traditional cassettes. A use of an existing rotating mechanism for the carrier assembly inside the chamber also provided improved film uniformity.

2.2 Film Thickness Measurement and Adhesion Quality

A physical scanning method was used to measure the coating thickness after deposition. The parylene film must first be patterned to create an edge for the actual measurement of a step height. In this quick and crude patterning preparation process, a Kapton masking tape was placed across a silicon test sample wafer before the parylene CVD process. After the parylene film deposition process, a sharp razor blade was used to carefully cut the parylene film along the edges of the Kapton tape. When the underlying tape was finally lifted, it carried away only the parylene portion above it, leaving the rest of the adjoining film adhering to the surface of the wafer. The adjoining film left a physical step imprint that could be used for thickness measurement. Care was exercised during peeling of the tape and film so as not to leave any rough edges that could distort the step height measurement. Films with good adhesion to the substrate did not show signs of lifting at the edges.

The film thickness was measured using an Ambios model 200 surface profilometer. An extremely lightweight needle, a.k.a a stylus, traveled across the patterned film edge and produced a step height trace measurement. Because the parylene film was a relatively soft material, a

lightweight stylus force setting of 0.05 mg force prevented any film indentation, which could have led to false readings. Even with the low vertical stylus force, a faint mark from the 2.5-micron radius tip stylus was visible on the film surface. A larger stylus tip radius would have been preferable, but one was not available at the time this work was done.

Surface traced profiles can also indicate problematic adhesion qualities of the parylene film to different types of surfaces. We performed the tape lifting test on silicon and silicon dioxide substrates. The plot in Fig. 5a was obtained from a 10-micron-thick parylene film in good contact with a silicon surface sample. The trace along the parylene surface is parallel to the silicon surface until the edge. The edge of the parylene is well anchored to the silicon surface and no lifting occurred at the edge. Figure 5b shows an example of poor adhesion on a different material sample, in this case, silicon dioxide. The trace along the parylene film was not parallel and there was rise in the traced profile near the edge instead of a natural drop in the slope, showing poor film adhesion on a silicon dioxide surface. Although the rise exceeded the plotted scale of 20 microns, the stylus completed a detailed trace of the surface-lifting features. We explain ways of improving parylene adhesion on any material in section 2.3.

The observed wavy surface trace above the parylene film may have been caused by the frictional drag of the stylus as it travelled across the film surface. A trace beyond the parylene step edge into the silicon or silicon dioxide substrate side shows no waviness. A wide band of gray-shaded markers appearing on both sides of the figure represents arbitrarily positioned markers that aid in averaging the surface perturbations during the measurement and height calculations. The gray-shaded band marker represents 50 data points.

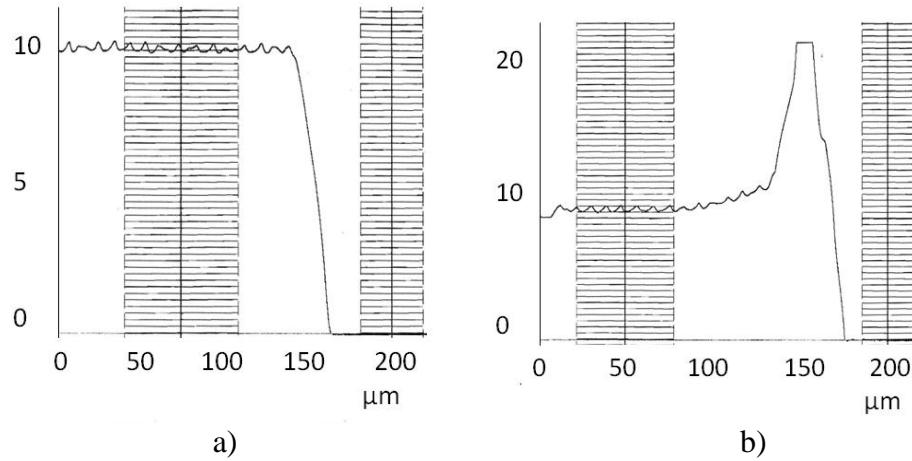


Fig. 5 Trace image of patterned parylene film edge indicating a) good and b) poor adhesion

2.3 Film Adhesion Promoter and Release Agent

Different substrate materials require surface preparation for improved parylene film adhesion. Parylene films are hydrophobic and will generally adhere well to other hydrophobic surfaces such as a clean, bare silicon surface. However, hydrophilic surfaces, such as silicon dioxide,

require the use of an adhesion promoter to ensure good adhesion between the parylene film and the surface. Thus, a widely used adhesion promoter, Silane A-174, was applied to the surface of the sample just prior to placing it in a parylene coater.

From the equipment point of view, it is desirable to reduce the buildup and eventually remove the deposited parylene film from the chamber. Thus, the internal surface chambers were treated with a release agent, such as a solution of diluted Micro-90 or equivalent. Release agents were routinely used on the unheated internal parts of the deposition chamber to promote easier cleaning of the thick parylene buildup after several deposition runs.

2.4 Temperature Gradients

Temperature gradients inside the chamber during long runs are a concern because any fluctuation beyond ambient conditions may inadvertently trigger a response in the nanoenergetic material being coated. Experiments have determined that a reaction between PS and an oxidizer can start at temperatures as low as 250 °C. Although the chamber is supposed to be at room temperature, a short tube connects the chamber to the adjacent pyrolysis furnace, which is set at 175 °C. So while a short deposition time of 1 h had no immediate effect on the sample, the longer 3-h depositions were a concern. Therefore, temperature measurements were performed on the external metal chamber walls during actual deposition runs using an infrared thermometer to characterize the thermal environment. Also, a temperature reading was taken of the substrate carrier bed inside the chamber immediately following a run. The resulting temperature was 25 °C for 1-h deposition run times, but on longer runs, the maximum temperature reached was 52 °C near the exit port of the pyrolysis furnace and 32 °C near the exhaust port of the chamber. Finally, a temperature measurement of 46 °C was recorded in the middle of the carrier immediately after its removal from the chamber. These experimental runs determined that existing temperature gradients should not be of concern for most applications unless a process calls for absolute room temperature.

2.5 Film Characterization and Prediction

We also found the coating thickness of a parylene film depended on the location of the wafer in the carrier apparatus. The resultant film thicknesses for several wafers distributed on different levels of the modified holding apparatus for a 25-g dimer run are shown in Table 1. We verified that the dimer was completely consumed at the end of the run. The carrier height is approximately 10 in, but divided into 16 levels, the top having the lowest labeled number. Thickness measurements of the deposited film were taken from the center as well as the edge of the 100-mm-diameter wafers. Not all wafer levels were measured.

Table 1 Coating thickness according to the level height on the wafer holding apparatus

Apparatus Level No.	Parylene Film Thickness (μm)	
	Center of Wafer	Edge of Wafer
2	6.60	6.74
4	6.00	6.24
6	5.74	6.00
7	5.73	5.94
8	5.73	6.00
9	5.73	5.82
11	5.67	5.70
13	5.27	5.64
14	5.25	5.56
16	4.65	4.90

It is evident from the results in the table that there was a decrease in coating thickness in wafers located from top to bottom of the carrier apparatus. The data suggest that the parylene vapor is more concentrated toward the top of the chamber. A baffle on the exit side of the pyrolysis tube where it connects to the chamber helps distribute the vapor uniformly across the chamber, but as can be seen from Table 1, that baffle is not totally effective in preventing non-uniformities from top to bottom. Although the thickness change from top to bottom is about 30%, the central positions 6 through 11 of the carrier show very good uniformity. Additionally, in the central region of the carrier apparatus, each wafer has only a 0.25- μm variation from edge to center. We also observed the thickness is greater at the edge of the wafer, suggesting that the parylene vapor depletes toward the center during the coating process.

Finally, we developed a chart for predicting film thickness based on the amount of parylene dimer loaded into the vapor chamber. Figure 6 shows a plot of parylene film thickness versus the starting dimer weight. The data were obtained from level 8 of the carrier. Although the plot shows a deviation from a straight line, the relationship is reproducible from run to run and does not change whether or not the carrier apparatus is partially or completely filled to capacity.

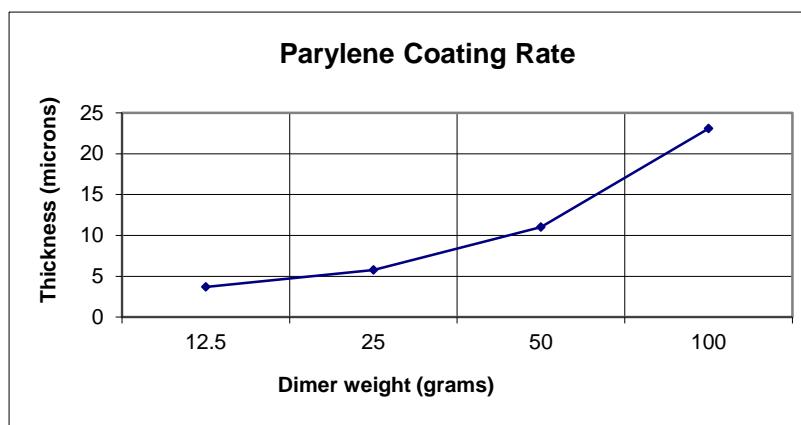


Fig. 6 Chart for predicting final parylene film thickness based on dimer weight

2.6 Hermetic Encapsulation of Nanoenergetic Device

Characterization of silicon for nanoenergetic PS applications has been described previously.^{3,4} When a silicon fuel source is combined with an oxidant on the nanoscale, the kinetic limitations of silicon oxidation are overcome and an energetic reaction is realized. Gas adsorption measurements and gravimetric techniques have determined the diameter of silicon pores to be in the range of 1–5 nm depending on the hydrogen fluoride (HF)/ethanol etching mixture concentration, electrolytic current, and etching time. A moisture barrier over a nanoporous etched silicon device for energetic applications is needed in high moisture environments because of the hygroscopic nature of the oxidizer. Parylene films are generally known to be impervious to moisture and liquids, which make them attractive for hermetic sealing and can improve the reliability and repeatability of the kinetic reactions in these devices.

Prior to sealing the PS and applying the oxidizer to activate the device, an atomic force microscope (AFM) model Veeco NanoMan V was used to determine the surface roughness of nanoporous silicon samples. AFM can provide detailed surface analysis data, illustrate surface changes on the nanometer scale, and measure average roughness (Ra) readings. Silicon samples were etched in HF/ethanol mixture for 5 and 45 min. AFM images of nanoporous silicon surface are illustrated in Fig. 7 with a) Ra of 0.11 nm due to 5 min of etching and b) Ra of 0.26 nm due to 45 min of etching. A difference between the shortest and longest etching time, the equivalent of 9 times, only increased the average roughness by 2.4 times. The sample etched for 45 min shows evidence of indentations on the surface. Analysis from a cross-sectional view map of the scan (not shown here) indicates the indentation has a diameter of approximately 30 nm. The AFM provided a detailed illustration of the nanoporous silicon and demonstrated the different surface characteristics that resulted from the etching and processing conditions.

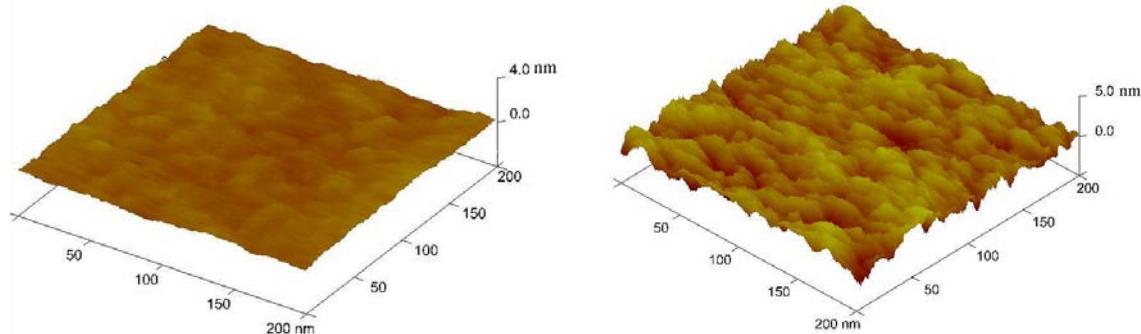


Fig. 7 AFM images of nanoporous silicon features with a) Ra of 0.11 nm due to 5 min of etching and b) Ra of 0.26 nm due to 45 min of etching.

After preparation of the nanoporous silicon, an aqueous oxidizer, sodium perchlorate (NaClO_4) in ethanol, was applied to fill the pores, allowed to dry, and followed by a coating of parylene film. The NaClO_4 solution is hygroscopic in nature and tends to absorb moisture from the

atmosphere and must be coated with a barrier to extend the device shelf life, otherwise the device will not repeatedly activate with the same exothermic output when activated by a hot wire.

Figure 8 shows a patterned device after hermetic encapsulation by parylene. The dark patterned circle represents nanoporous etched silicon region with gold patterned electrical hot wire running across. The white residue represents excess oxidizer, and a transparent parylene encapsulation layer is lastly applied to prevent moisture absorption. Methods to improve the mixture of NaClO_4 , its uniform coating, and residue characteristics on the surface of the device are under way.

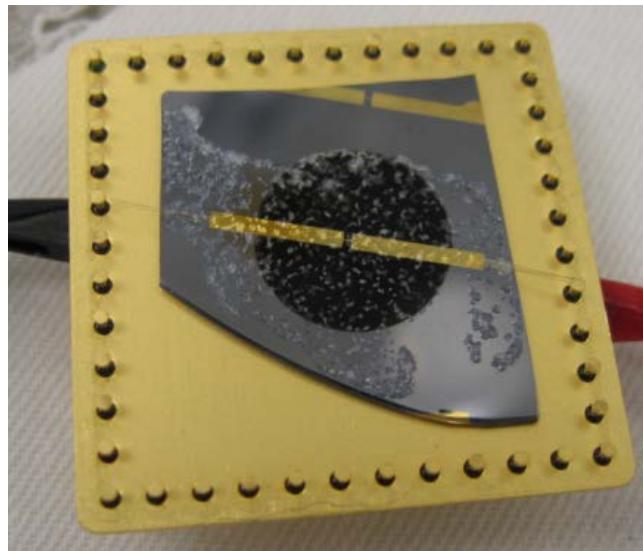


Fig. 8 Device mounted on a wire-bonded package showing circular etched nanoporous silicon in black color and patterned electrical wire in gold color. The white residue represents excess oxidizer covered by a transparent parylene encapsulation layer.

The parylene coating process is considered to be a room temperature controlled technique. No exothermic chemical reaction occurred between NaClO_4 and silicon during the room temperature deposition process. The parylene coating was transparent with good adhesion qualities and showed no evidence of lifting or pealing from the wafer surface. We tested the adequacy of the coated device with parylene protection and found the shelf life and energetic output is repeatable beyond 15 h in very high moisture environments.

3. Conclusions

Parylene films were deposited with good physical properties and thickness repeatability using the procedures described in this report. The films show very good uniformity across a 100-mm-diameter wafer surface and from wafer to wafer within the centrally located sections of the wafer carrier. With proper maintenance of the parylene system and adjustment of the

deposition procedure, the deposited films were also clear and free of any cloudiness, particles, or bubbling. We have also demonstrated repeatable nanoenergetic PS device performance beyond 15 h with parylene encapsulation. AFM provided measurements of average surface roughness and is an excellent tool for surface analysis.

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